T0021F" 60T2E00F

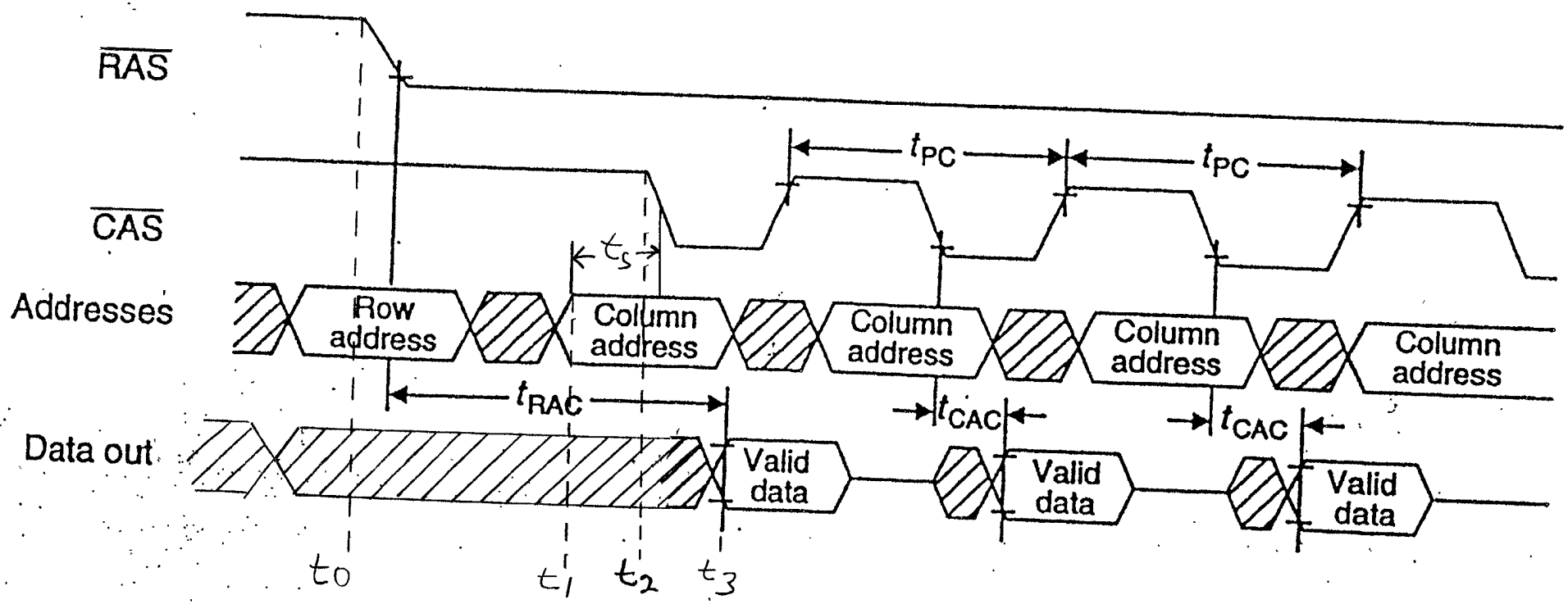


FIG. 1 (PRIOR ART)

T0022T* 60T26D0T

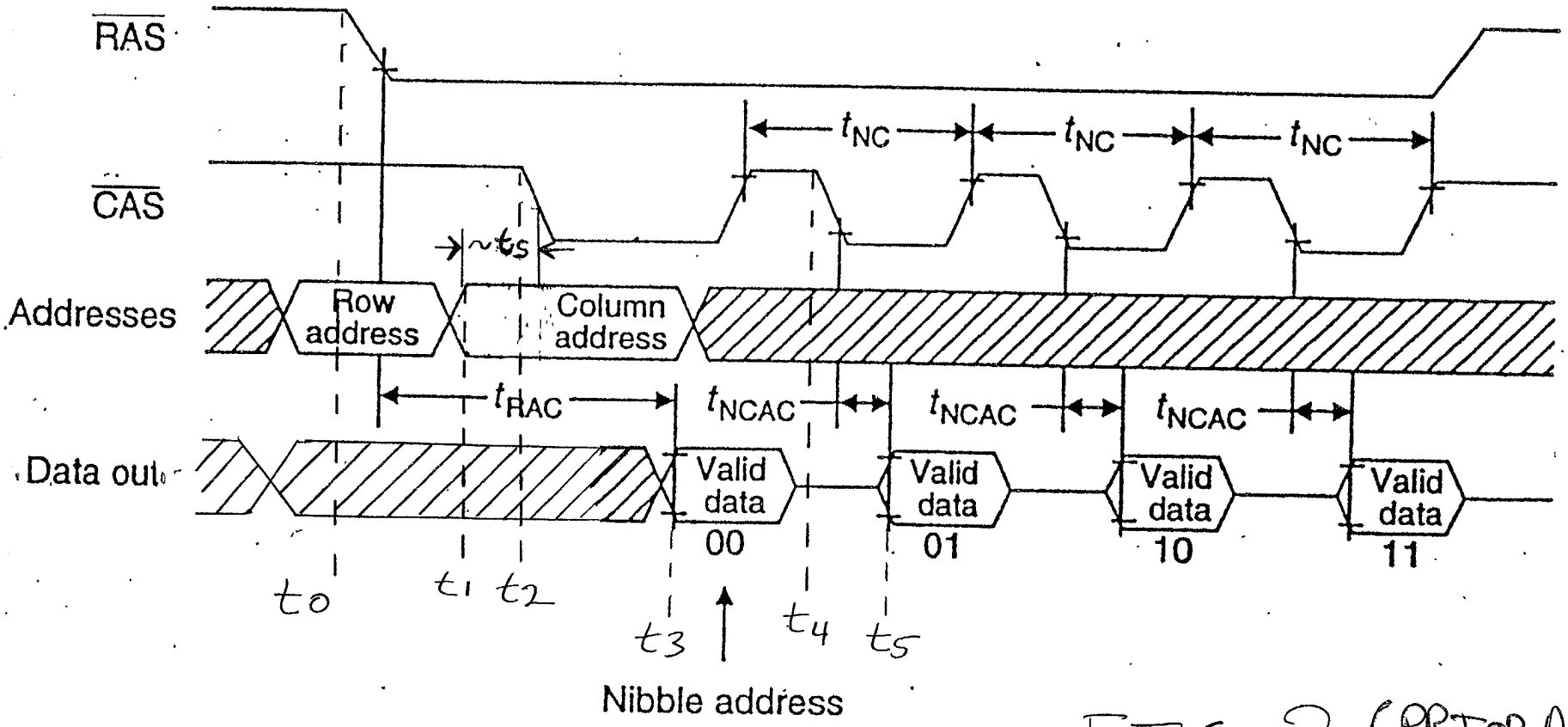


FIG. 2 (PRIOR ART)

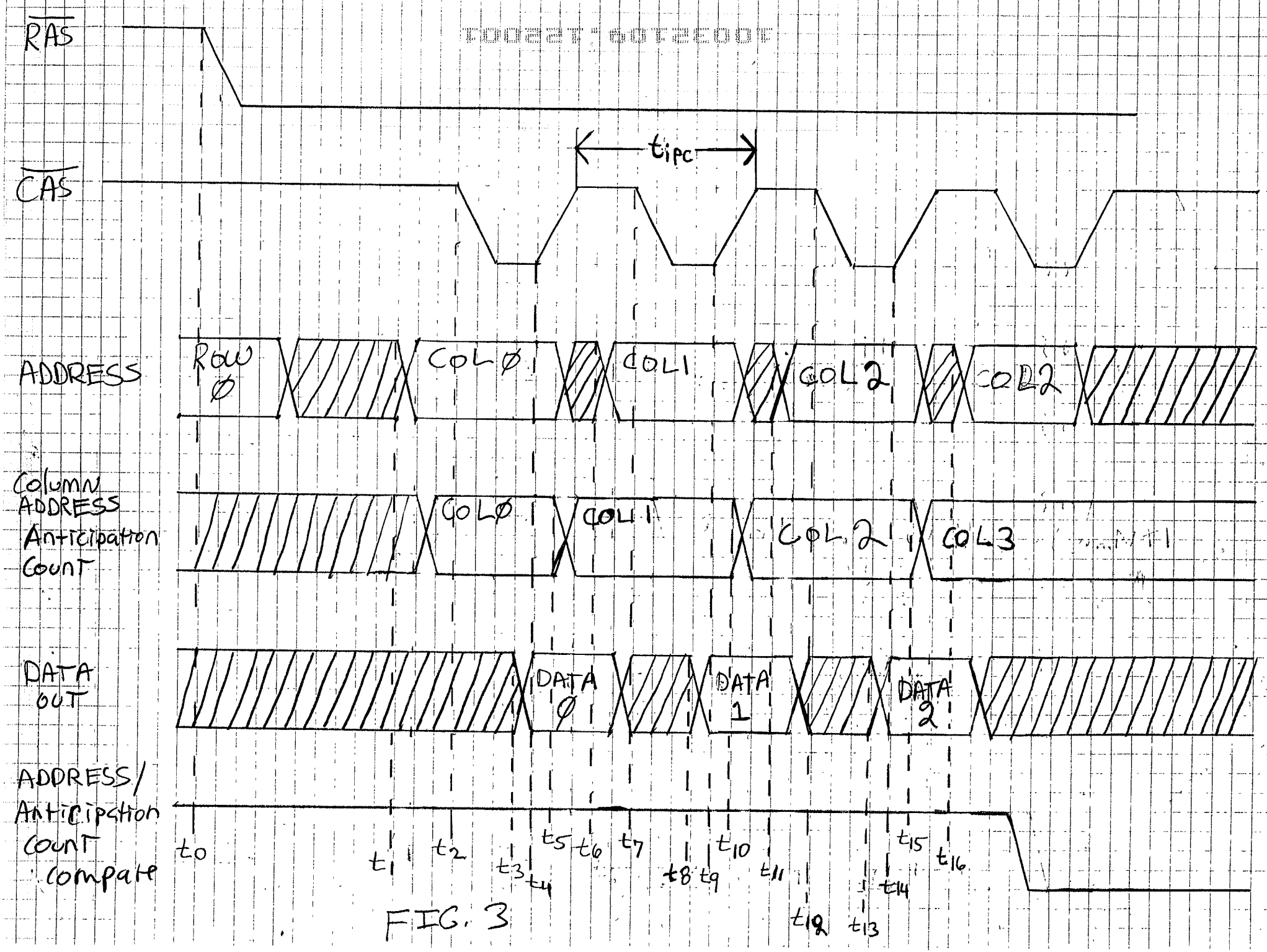
RAS
CAS
$t_{PC}$
ADDRESS
ROW Ø
COL Ø
COL 1
COL 2
COL 2
Column Address Anticipation Count
COL Ø
COL 1
COL 2
COL 3
DATA OUT
DATA Ø
DATA 1
DATA 2
ADDRESS/ Anticipation Count Compare
$t_0$
$t_1$
$t_2$
$t_3$
$t_4$
$t_5$
$t_6$
$t_7$
$t_8$
$t_9$
$t_{10}$
$t_{11}$
$t_{12}$
$t_{13}$
$t_{14}$
$t_{15}$
$t_{16}$

FIG. 3

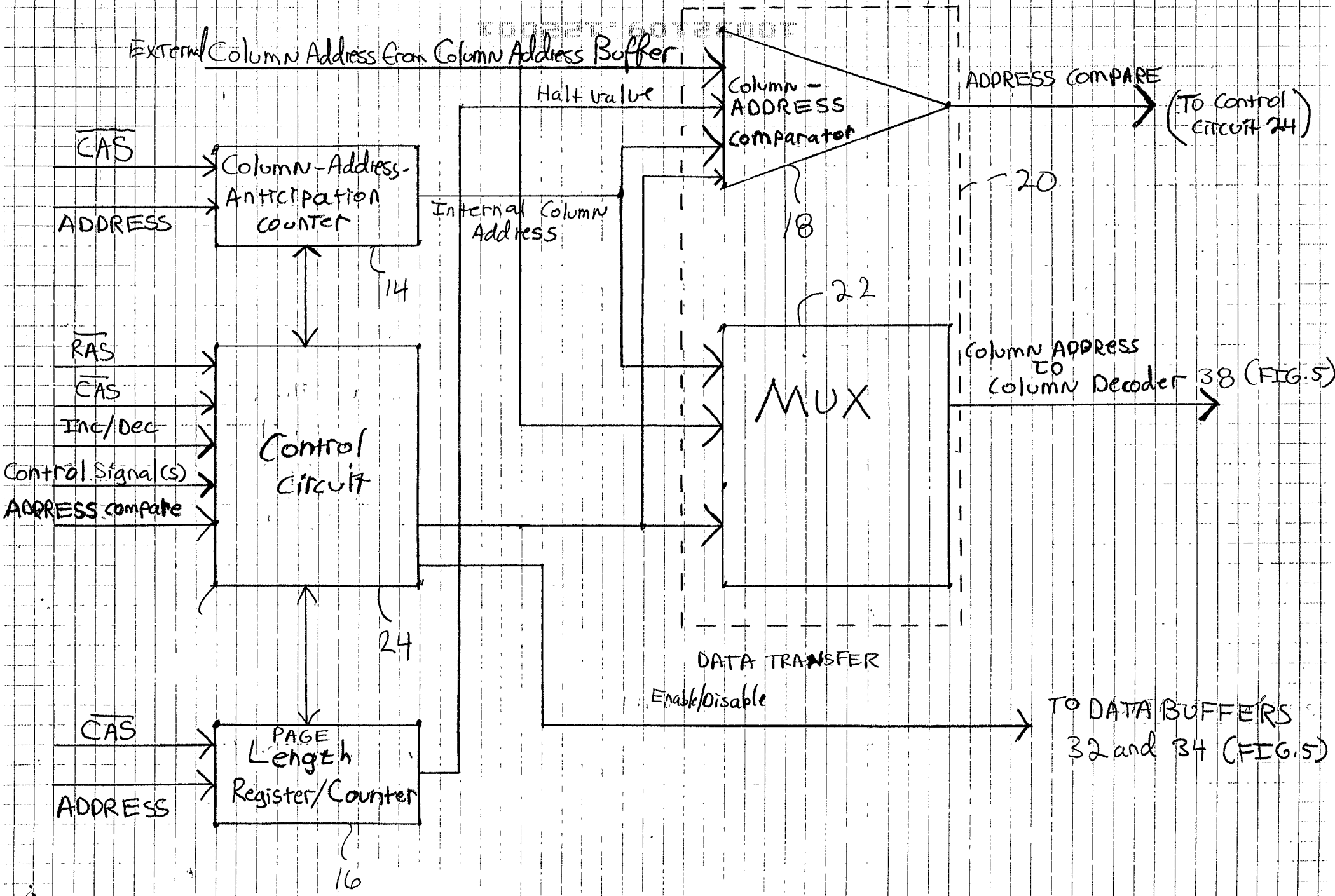
External Column Address from Column Address Buffer
Halt value
Column-ADDRESS comparator
ADDRESS COMPARE
(To Control Circuit 24)
18
20
CAS
ADDRESS
Column-Address-Anticipation counter
Internal Column Address
14
22
RAS
CAS
Inc/Dec
Control Signal(s)
ADDRESS compare
Control Circuit
MUX
Column ADDRESS to Column Decoder 38 (FIG. 5)
24
DATA TRANSFER Enable/Disable
TO DATA BUFFERS 32 and 34 (FIG. 5)
CAS
ADDRESS
PAGE Length Register/Counter
16

FIG. 4

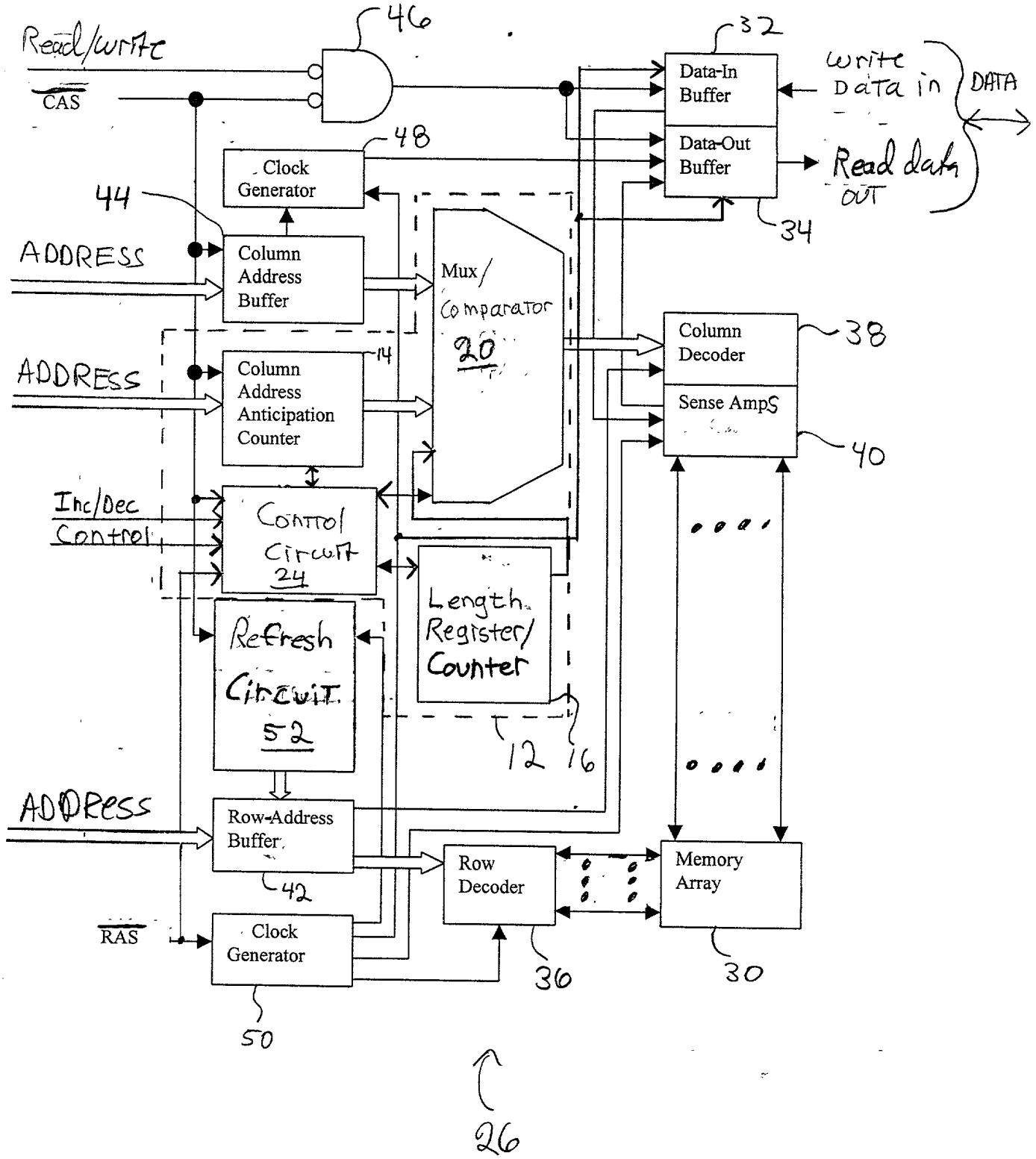
Read/write
CAS
46
32
Data-In Buffer
Data-Out Buffer
write Data in
DATA
Read data OUT
34
48
Clock Generator
44
ADDRESS
Column Address Buffer
Mux/ Comparator 20
ADDRESS
Column Address Anticipation Counter
14
Column Decoder
38
Sense Amps
40
Inc/Dec Control
Control Circuit 24
Length Register/ Counter
Refresh Circuit 52
12
16
ADDRESS
Row-Address Buffer
42
Row Decoder
Memory Array
RAS
Clock Generator
50
36
30
26

FIG. 5

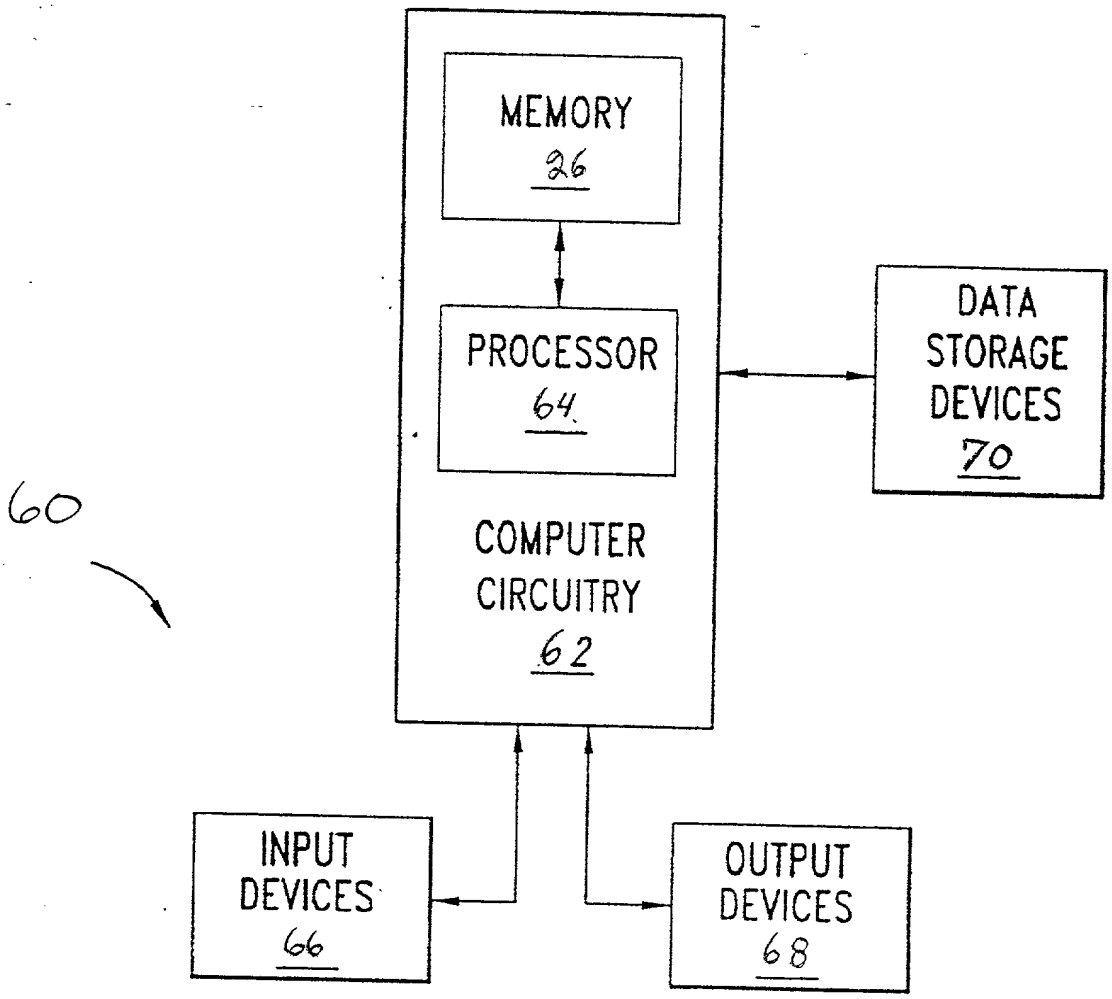
60
MEMORY
26
PROCESSOR
64
COMPUTER
CIRCUITRY
62
DATA
STORAGE
DEVICES
70
INPUT
DEVICES
66
OUTPUT
DEVICES
68

*Fig. 6*